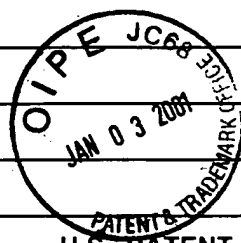


INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)



Atty. Docket No.	03180.0265	Serial No.	09/661,919
Applicant	Taku UCHINO		
Filing Date	January 3, 2001	Group	2816

U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Date	Name	Class	Sub Class	Filing Date If Appropriate
<i>72</i>	5,966,523	10/12/99	Uchino			
<i>72</i>	5,847,966	12/08/98	Uchino et al.			

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Document Number	Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>72</i>	NAJM et al.; "Probabilistic Simulation for Reliability Analysis of CMOS VLSI Circuits", IEEE Transactions on Computer-Aided Design, VOL. 9, NO. 4, pp. 439-450, (1990)
<i>72</i>	TSUI et al.; "Efficient Estimation of Dynamic Power Consumption Under a Real Delay Model", International Conference on Computer-Aided Design, pp. 224-228, (1993)
<i>72</i>	UCHINO et al.; "Switching Activity Analysis using Boolean Approximation Method", International Conference on Computer-Aided Design, pp. 20-25, (1995)

Examiner <i>72</i>	Date Considered <i>5/7/04</i>
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INFORMATION DISCLOSURE CITATION	Atty. Docket No.	Serial No.
	3180.0265	09/661,919
	Applicant	
	Uchino	
	Filing Date	Group
	September 14, 2000	2816

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*Examiner Initial	Document Number	Date	Country	Class	Sub- Class	Translation	
						Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

702	Copy of U.S. Patent Application Serial No. 09/312,828
	NOW US PATENT # 6,272,683

Examiner <u>702</u>	Date Considered <u>5/7/04</u>
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